

## In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Previously Presented) A multiply-accumulate module  
2 comprising:  
3 a multiply-accumulate core, wherein said multiply-accumulate  
4 core comprises:  
5 a plurality of Booth encoder cells;  
6 a plurality of Booth decoder cells connected to at least  
7 one of said Booth encoder cells, said plurality of Booth decoder  
8 cells including at least one first Booth decoder cell and at least  
9 one second Booth decoder cell, said at least one first Booth  
10 decoder cell structurally the same as said at least one second  
11 Booth decoder cells; and  
12 a plurality of Wallace tree cells connected to at least  
13 one of said Booth decoder cells, said plurality of Wallace tree  
14 cells including at least one first Wallace tree cell and at least  
15 one second Wallace tree cell, said at least one first Wallace tree  
16 cell structurally the same as said at least one second Wallace tree  
17 cell;  
18 wherein said multiply-accumulate module includes at least one  
19 critical path, said at least one critical path being an electrical  
20 path for which an amount of time that it takes for an electrical  
21 signal to travel from an input of said multiply-accumulate core to  
22 an output of said multiply-accumulate core is greater than or equal  
23 to a predetermined amount of time and less than a longest amount of  
24 time that it takes any other electrical signal to travel from said  
25 input of said multiply-accumulate core to said output of said  
26 multiply-accumulate core, wherein said predetermined amount of time  
27 is less than said longest amount of time;

28            wherein said at least one first Wallace tree cell or said at  
29   least one first Booth decoder cell are disposed on said at least  
30   one critical path;

31            wherein said at least one second Wallace tree cell and said at  
32   least one second Booth decoder cell are not disposed on any of said  
33   at least one critical path;

34            wherein said at least one first Wallace tree cell or said at  
35   least one first Booth decoder cell comprises a first plurality of  
36   transistors, and at least one second Wallace tree cell or at least  
37   one second Booth decoder cell comprises a second plurality of  
38   transistors; and

39            a width of at least one of said first plurality of transistors  
40   of said at least one first Wallace tree cell or said at least one  
41   first Booth decoder cell is greater than a width of a corresponding  
42   one of said second plurality of transistors of a corresponding one  
43   of said at least one second Wallace tree cell and said at least one  
44   second Booth decoder cell.

2.    (Canceled)

1    3.    (Previously Presented) The multiply-accumulate module of claim  
2    1, wherein said multiply-accumulate core further comprises:

3            an adder connected to at least one of said Wallace tree cells;  
4            a saturation detector connected to said adder, wherein said  
5   multiply-accumulate module further comprises:

6            at least one input register connected to at least one of said  
7   Booth encoding cells; and

8            at least one result register connected to said saturation  
9   detector.

4 to 8.    (Canceled)

1 9. (Original) The multiply-accumulate module of claim 1, wherein  
2 said at least one second cell is a most significant bit or a least  
3 significant bit and said at least one first cell is not a most  
4 significant bit or a least significant bit.

1 10. (Previously Presented) A parallel multiplier comprising:  
2 a parallel multiplier core, wherein said parallel multiplier  
3 core comprises:

4 a plurality of Booth encoder cells;  
5 a plurality of Booth decoder cells connected to at least  
6 one of said Booth encoder cells, said plurality of Booth decoder  
7 cells including at least one first Booth decoder cell and at least  
8 one second Booth decoder cell, said at least one first Booth  
9 decoder cell structurally the same as said at least one second  
10 Booth decoder cells; and

11 a plurality of Wallace tree cells connected to at least  
12 one of said Booth decoder cells, said plurality of Wallace tree  
13 cells including at least one first Wallace tree cell and at least  
14 one second Wallace tree cell, said at least one first Wallace tree  
15 cell structurally the same as said at least one second Wallace tree  
16 cell;

17 wherein said multiply-accumulate module includes at least one  
18 critical path, said at least one critical path being an electrical  
19 path for which an amount of time that it takes for an electrical  
20 signal to travel from an input of said multiply-accumulate core to  
21 an output of said multiply-accumulate core is greater than or equal  
22 to a predetermined amount of time and less than a longest amount of  
23 time that it takes any other electrical signal to travel from said  
24 input of said multiply-accumulate core to said output of said  
25 multiply-accumulate core, wherein said predetermined amount of time  
26 is less than said longest amount of time;

27            wherein said at least one first Wallace tree cell or said at  
28   least one first Booth decoder cell are disposed on said at least  
29   one critical path;

30            wherein said at least one second Wallace tree cell and said at  
31   least one second Booth decoder cell are not disposed on any of said  
32   at least one critical path;

33            wherein said at least one first Wallace tree cell or said at  
34   least one first Booth decoder cell comprises a first plurality of  
35   transistors, and at least one second Wallace tree cell or at least  
36   one second Booth decoder cell comprises a second plurality of  
37   transistors; and

38            a width of at least one of said first plurality of transistors  
39   of said at least one first Wallace tree cell or said at least one  
40   first Booth decoder cell is greater than a width of a corresponding  
41   one of said second plurality of transistors of a corresponding one  
42   of said at least one second Wallace tree cell and said at least one  
43   second Booth decoder cell.

11. (Canceled)

1   12. (Previously Presented) The parallel multiplier of claim 10,  
2   wherein said parallel multiplier core further comprises:

3          an adder connected to at least one of said Wallace tree cells;  
4          a saturation detector connected to said adder, wherein said  
5   parallel multiplier further comprises:

6          at least one input register connected to at least one of said  
7   Booth encoding cells; and

8          at least one result register connected to said saturation  
9   detector and at least one of said Wallace tree cells.

13 to 17. (Canceled)

1 18. (Original) The multiply-accumulate module of claim 10, wherein  
2 at least one second cell is a most significant bit or a least  
3 significant bit and at least one first cell is not a most  
4 significant bit or a least significant bit.

1 19. (Previously Presented) A method of designing a multiply-  
2 accumulate module comprising the steps of:  
3 providing a multiply-accumulate core, wherein the step of  
4 providing a multiply-accumulate core comprises the steps of:  
5 providing a plurality of Booth encoder cells;  
6 connecting a plurality of Booth decoder cells to at least  
7 one of said Booth encoder cells;  
8 connecting a plurality of Wallace tree cells to at least  
9 one of said Booth decoder cells;  
10 defining at least one critical path within said multiply-  
11 accumulate module, said at least one critical path being an  
12 electrical path for which an amount of time that it takes for an  
13 electrical signal to travel from an input of said multiply-  
14 accumulate core to an output of said multiply-accumulate core is  
15 greater than or equal to a predetermined amount of time and less  
16 than a longest amount of time that it takes any other electrical  
17 signal to travel from said input of said multiply-accumulate core  
18 to said output of said multiply-accumulate core, wherein said  
19 predetermined amount of time is less than ~~a~~ said longest amount of  
20 time;  
21 defining a Wallace tree cell disposed on said at least  
22 one critical path as a first Wallace tree cell;  
23 defining a Wallace tree cell not disposed on any of said  
24 at least one critical path as second Wallace tree cell;  
25 defining a Booth decoder cell disposed on said at least  
26 one critical path as a first Booth decoder cell;

27           defining a Booth decoder cell not disposed on any of said  
28 at least one critical path as second Booth decoder cell;  
29           constructing each first Wallace tree cell and each first  
30 Booth decoder cell of a first plurality of transistors, each first  
31 Wallace tree cell structurally the same as each second Wallace tree  
32 cell, and constructing each second Wallace tree cell and each  
33 second Booth decoder cell of a second plurality of transistors,  
34 each first Booth decoder cell structurally the same as each second  
35 Booth decoder cell;  
36           selecting a first width for at least one of said first  
37 plurality of transistors of at least one of said first Wallace tree  
38 cell or said first Booth decoder cell; and  
39           selecting a second width for at least one of said second  
40 plurality of transistors of a second Wallace tree cell  
41 corresponding to said at least one of said first Wallace tree cell  
42 or of a second Booth decoder cell corresponding to said first Booth  
43 decoder cell which is less than said first width of a corresponding  
44 one of said first plurality of transistors.

1   20. (Previously Presented) A method of designing a parallel  
2 multiplier comprising the steps of:  
3       providing a parallel multiplier core, wherein the step of  
4 providing a parallel multiplier core comprises the steps of:  
5           providing a plurality of Booth encoder cells;  
6           connecting a plurality of Booth decoder cells to at least  
7 one of said Booth encoder cells;  
8           connecting a plurality of Wallace tree cells to at least  
9 one of said Booth decoder cells;  
10       defining at least one critical path within said multiply-  
11 accumulate module, said at least one critical path being an  
12 electrical path for which an amount of time that it takes for an  
13 electrical signal to travel from an input of said multiply-

14 accumulate core to an output of said multiply-accumulate core is  
15 greater than or equal to a predetermined amount of time and less  
16 than a longest amount of time that it takes any other electrical  
17 signal to travel from said input of said multiply-accumulate core  
18 to said output of said multiply-accumulate core, wherein said  
19 predetermined amount of time is less than a said longest amount of  
20 time;

21         defining a Wallace tree cell disposed on said at least  
22 one critical path as a first Wallace tree cell;

23         defining a Wallace tree cell not disposed on any of said  
24 at least one critical path as second Wallace tree cell;

25         defining a Booth decoder cell disposed on said at least  
26 one critical path as a first Booth decoder cell;

27         defining a Booth decoder cell not disposed on any of said  
28 at least one critical path as second Booth decoder cell;

29         constructing each first Wallace tree cell and each first  
30 Booth decoder cell of a first plurality of transistors, each first  
31 Wallace tree cell structurally the same as each second Wallace tree  
32 cell, and constructing each second Wallace tree cell and each  
33 second Booth decoder cell of a second plurality of transistors,  
34 each first Booth decoder cell structurally the same as each second  
35 Booth decoder cell;

36         selecting a first width for at least one of said first  
37 plurality of transistors of at least one of said first Wallace tree  
38 cell or at least one of said first Booth decoder cell; and

39         selecting a second width for at least one of said second  
40 plurality of transistors of a second Wallace tree cell  
41 corresponding to said at least one of said first Wallace tree cell  
42 or of a second Booth decoder cell corresponding to said first Booth  
43 decoder cell which is less than said first width of a corresponding  
44 one of said first plurality of transistors.